configured or pre-designed blocks, includes conductors that are routed independent from other circuits in the integrated circuit. The self contained layout section, which implement Manhattan wiring geometries, may utilize one or more wiring (*e.g.*, metal layers) of the integrated circuit. Diagonal wires are routed over the self contained layout section. The self contained layout section is not affected by the diagonal wires deposed on metal layers above them. The self contained layout section may incorporate memory circuits, small cells that implement simple logic functions, as well as large functional blocks that implement specific functionalities.

Rejection of the Claims Under 35 U.S.C. § 102 & § 103

In the Office Action dated January 3, 2002, claims 16-23, 25-35 and 37-39 were rejected under 35 U.S.C. § 102 as being anticipated by US Patent 6,262,487, issued to Igarashi *et al.* (hereafter referred to as "*Igarashi et al.*"). Claims 24 and 36 are rejected under 35 U.S.C. § 103 as being unpatentable over *Igarashi et al* in view of US Patent 5,635,736, issued to Funaki et al. (hereafter referred to as "*Funaki et al.*").

Overview of *Igarashi et al.* and *Funaki et al.*:

Igarashi et al. disclose an integrated circuit device and cell arranging method. Figure 20 of *Igarashi et al.* discloses a five layer wiring architecture. The first three layers comprise wires situated in the X-axis, Y-axis, and X-axis directions, respectively. The wires of the fourth and fifth layers are arranged in oblique directions (45 degrees), relative to the wires arranged in the first three layers.

Funaki et al. disclose wiring for a MOS gate type semiconductor device. Figure 1 shows a two-layer structure SD wiring pattern. The length wise direction of the drain electrode is oblique to the axis at 45 degrees. A drain electrode is symmetrical to another drain electrode with respect to a line in the y-axis direction formed at a position apart from that drain electrode in the x-axis. Thus, the drain electrodes constitute a "V" pattern separated at its center into two halves.

A. The References Do Not Disclose A Diagonal Direction Wiring Section Directly Adjacent To A Self Contained Layout Section.

Claim 16 sets forth the limitations:

a first metal layer group comprising at least one metal layer, said metal layer in said first metal layer group comprising a self contained layout section comprising conductors deposed in a preferred Manhattan direction, ... said self contained layout section comprising a routing of conductors, for a portion of said metal layer, developed independent from routing of conductors for circuits in said integrated circuit; and

a second metal layer group comprising at least one metal layer, said metal layer in said second metal layer group comprising a plurality of conductors deposed in a preferred diagonal direction in a portion of the metal layer directly adjacent to said portion of said metal layer for said self contained layout.

Claim 28 recites the limitations:

designating a first metal layer group comprising at least one metal layer, said metal layer in said first metal layer group comprising at least one self contained layout section comprising conductors deposed in a preferred Manhattan direction, wherein a preferred direction defines a direction, relative to the integrated circuit boundaries, for at least fifty percent of conductors and said self contained layout section comprising a routing of conductors, for a portion of said metal layer, developed independent from routing of conductors for circuits in said integrated circuit; and

designating a second metal layer group comprising at least one metal layer, said metal layer in said second metal layer group comprising a plurality of conductors deposed in a preferred diagonal direction in a portion of the metal layer directly adjacent to said portion of said metal layer for said self contained layout.

Applicants respectfully contend that the cited references fail to disclose or teach toward a wiring architecture with a self contained layout in a first metal layer group, with wires arranged in a Manhattan direction, and conductors, from a second metal layer group, arranged in a diagonal direction in a portion of the metal layer directly adjacent to the portion of the metal layer for the self contained layout.

Igarashi et al. do not disclose conductors, arranged in a Manhattan direction, for "a portion of said metal layer" as claimed in claims 16 and 28. Instead, *Igarashi et al.*

disclose Manhattan directional conductors for the entire layer (*e.g.*, the first three layers for the embodiment of Figure 20). *Funaki et al.* do not disclose Manhattan directional wiring. Accordingly, *Igarashi et al.* and *Funaki et al.* do not anticipate claims 16 and 28.

B. The Cited References Do Not Disclose Wiring Architectures Suitable For Self Contained Layout Sections.

Neither *Igarashi et al.* nor *Funaki et al.* disclose techniques for handling self contained wiring sections. The techniques of the claimed invention provide noise immunity from Manhattan wiring geometries. The use of diagonal wiring in the present invention permits routing wires in areas above IP blocks (*e.g.*, self contained wiring sections). Since the IP blocks utilize Manhattan wiring geometries, the use of diagonal wires in metal layers above the IP blocks do not result in noise coupling between the wires on the metal layer(s) and the wires on the IP block.

The claimed invention supports a hierarchical design approach. In a hierarchical design approach, wires in a subsection of the IC are routed independent of other areas of the IC. For example, an IP block, which includes Manhattan directional wires routed independent of other portions of the IC, may be integrated into an IC employing diagonal wires without noise coupling concerns.

Dependent Claims:

Dependent claims 17-27 are depend, either directly or indirectly, upon independent claim 16, and therefore for the same reasons claim 1 is patentable over the cited references, claims 17-27 are also patentable over the references. Similarly, claims 29-39 are directly or indirectly, dependent, upon claim 28, and therefore for the same reasons claim 28 is patentable over the cited references, claims 29-39 are also patentable over the references.

CONCLUSION

In view of the foregoing, it is submitted that the claims are in condition for allowance. Reconsideration of the rejections and objections is requested. Allowance is earnestly solicited at the earliest possible date.

Respectfully submitted,

STATTLER JOHANSEN & ADELI LLP

Dated: 6/3/02

John Stattler
Reg. No. 36,285

Stattler, Johansen & Adeli LLP
PO Box 51860
Palo Alto, CA 94303-0728
Phone: (650) 752-0990 ext.100
Fax: (650) 752-0995

The Amended Claims ✓

The following pages provide the amended claims with the amendments marked with deleted material in [brackets] and new material underlined to show the changes made.

16. (Once Amended) An integrated circuit comprising:

a plurality of metal layers comprising a plurality of conductors to interconnect components in [said] an integrated circuit, said metal layers comprising:

a first metal layer group comprising at least one metal layer, said metal layer in said first metal layer group comprising at least one self contained layout section comprising conductors deposed in a preferred Manhattan direction, wherein a preferred direction defines a direction, relative to the integrated circuit boundaries, for at least fifty percent of conductors, and said self contained layout section comprising a routing of conductors, for a portion of said metal layer, developed independent from routing of conductors for circuits in said integrated circuit; and

a second metal layer group comprising at least one metal layer, said metal layer in said second metal layer group comprising a plurality of conductors deposed in a preferred diagonal direction in a portion of the metal layer directly adjacent to said portion of said metal layer for said self contained layout section.

28. (Once Amended) A method for deposing a plurality of metal layers comprising a plurality of conductors to interconnect components of an integrated circuit, said method comprising the steps of:

designating a first metal layer group comprising at least one metal layer, said metal layer in said first metal layer group comprising at least one self contained layout section comprising conductors deposed in a preferred Manhattan direction, wherein a preferred direction defines a direction, relative to the integrated circuit boundaries, for at least fifty percent of conductors and said self contained layout section comprising a routing of conductors, for a portion of said metal layer, developed independent from routing of conductors for circuits in said integrated circuit; and

designating a second metal layer group comprising at least one metal layer, said metal layer in said second metal layer group comprising a plurality of conductors deposed in a preferred diagonal direction in a portion of the metal layer directly adjacent to said portion of said metal layer for said self contained layout.

The Amended Specification

On page 1, line 3, after "Serial No.", please insert --09/733,104--.